Docket No.: 50432-593 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Lynn OKADA, et al.	:	Confirmation Number: 1080
Serial No.: 10/728,774	:	Group Art Unit: 2823
Filed: December 8, 2003	:	Examiner: Estrada, Michelle

For: SEALING SIDEWALL PORES IN LOW-K DIELECTRICS

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed May 4, 2006. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 AJS:ntb
Date: May 11, 2006

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APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed May 4, 2006, wherein Appellants appealed from the Primary Examiner's rejection of claims 1 through 3, 8 and 9.

I. REAL PARTY IN INTEREST

The Real Party In Interest is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related Appeal or Interference.

III. STATUS OF CLAIMS

Claims 1 through 6, 8 and 9 are pending in this Application. Claims 4 through 6 have been allowed. Claims 1 through 3, 8 and 9 have been rejected no less than four times, the most recent rejection being imposed in the Office Action dated April 14, 2006. It is from the multiple rejections of claims 1 through 3, 8 and 9 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the issuance of the Office Action dated April 17, 2006, wherein claims 1 through 3, 8 and 9 were rejected for the fourth time.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1, the only independent claim on appeal, is directed to a method of manufacturing a semiconductor device. The claimed method comprises the manipulative steps of forming an opening in a porous dielectric layer comprising a first low-k material (Fig. 2B; paragraph [24], lines 2, 5 and 6), the opening defined by sidewalls having exposed pores (Fig. 2B; paragraph [24], lines 7 and 8), sealing the exposed pores in the sidewalls by deposing a swelling agent lining the sidewalls (Fig. 2C; paragraph [24], lines 10 and 11), heating to swell the porous dielectric layer (paragraph [24], lines 11 and 12), and depositing a barrier metal lining the opening (Fig. 2E; paragraph [24], lines 13 and 14).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 through 3, 8 and 9 stand rejected under 35 U.S.C. § 103 for obviousness predicated upon Besser et al. in view of Mahulikar et al.

VII. ARGUMENT

For the convenience of the Honorable Board of Patent Appeals and Interferences (the "Board"), Appellants do not separately argue the patentability of dependent claims 2, 3, 8 and 9. Accordingly, claims 2, 3, 8 and 9 stand or fall together with independent claim 1 as a group.

The Examiner's rejection of claims 1 through 3 and 8 under 35 U.S.C. § 103 for obviousness predicated upon Besser et al. in view of Mahulikar et al.

In the statement of the rejection the Examiner **admitted** that Besser et al., the primary reference, do **not** disclose sealing the exposed pores in the sidewalls by depositing a swelling agent lining the sidewalls and heating to swell the porous dielectric layer. Then, in one sentence, the Examiner makes three erroneous factual determinations as to the teachings of Mahulikar et al. Specifically, the Examiner erroneously determined that:

> Mahulikar et al. disclose sealing the exposed pores in the **sidewalls** by deposing a swelling agent swelling lining the **sidewalls** and **heating to swell** the **porous dielectric layer** (Col. 5, lines 1-7). (Page 2 of the April 17, 2006 Office Action, ultimate full paragraph; Emphasis supplied).

Armed with the above fictional facts, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the technique of Besser et al. by implementing the teachings of Mahulikar et al. The Examiner is wrong.

Clearly erroneous factual determinations.

Contrary to the Examiner's assertion, Mahulikar et al. neither disclose nor suggest:

(1). sealing exposed pores in any **sidewalls**;

(2). heating to **swell** a porous dielectric layer; or

(3). any **porous dielectric layer**.

Besser et al. disclose a **damascene** technique for forming interconnect structures in low dielectric constant (low-k) materials. In **damascene** processing, an opening is formed in a dielectric layer and a metal, such as copper, is deposited therein and planarized. This is far afield from Mahulikar et al. who are concerned with maximizing the breakdown voltage of an **electronic package** design with **circuitry deposited directed on an anodized layer of aluminum**. Adverting to Fig. 1, which represents prior art to Mahulikar, defects which reduce the breakdown voltage when circuitry is formed on anodized aluminum include the formation of intermetallics (16), surface defects 18 which are difficult to fill, and pores 20 which accumulate contaminants 22. One of the solutions offered by Mahulikar et al. is to deposit a dielectric polymer 30 (Fig. 2) which seals the surface, including the surface defects and pores. The deposited polymer is then cured by heating.

The Examiner, of course, is required to **specifically identify** features in a reference which are asserted to correspond to features of a claimed invention, and to **specifically identify** a source in the reference for the requisite motivation, particularly when the required features and source are **not apparent** as in the present case. *Smiths Industries Medical System v. Vital Signs Inc., 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999).* That burden has **not** been discharged. Simply put, it is **not** apparent and the Examiner did **not** identify where Mahulikar et al. disclose:

(1). sidewalls;

(2). a porous dielectric layer, as that term would have been understood by one having ordinary skill in the art particularly in the context of the primary reference to Besser et al. (anodized aluminum is not a porous dielectric layer, and certainly not a porous dielectric layer in which an opening is formed to implement damascene processing); and

(3). heating to swell a nonexistent porous dielectric layer (there is no apparent factual basis upon which to predicate the determination anodized aluminum is even capable of swelling).

Based upon the foregoing, it should be apparent that even **if** the applied references are combined as suggested by the Examiner, and Appellants submit that the Examiner did not establish the requisite fact-based motivation as explained *infra*, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).*

There is no motivation.

Initially, it should be apparent that the secondary reference to Mahulikar et al. relates to **non-analogous** art with respect to both the claimed invention and with respect to the primary reference to Besser et al. Both the present invention and the primary reference relate to **damascene** processing wherein interconnect structures formed in dielectric material having a low dielectric constant. The reference to Mahulikar et al., on the other hand, relates to **packaging**, and particularly, the formation of circuitry deposited directly on anodized aluminum by various types of techniques. The subject matter of Mahulikar et al. has nothing whatsoever to do with the subject matter of the present invention or the subject matter of Besser et al. There is no apparent technical or logical reason why one having ordinary skill in the art, confronted with any problems relating to damascene processing, i.e., forming an interconnect structure in a porous dielectric layer, would ever look to how electronic package designs are formed with circuitry deposited directly on anodized aluminum. This being the case, it cannot be presumed that one having ordinary skill in the art, confronted with any problem related to forming an interconnect structure in a porous low dielectric constant material, would have been aware of or would have even looked to Mahulikar et al. *In re Clay, 966 F.2d 656, 23 USPQ2d 1058 (Fed. Cir. 1992).*

Aside from the non-analogous art issue, Appellants submit that the Examiner did not establish the requisite fact-based motivation. Specifically, in order to establish the requisite fact-based motivation, the Examiner must make clear and particular factual findings as to a specific understanding or specific technological principle and then, based upon such facts, explain why one having ordinary skill in the art would have been realistically impelled to modify particular prior art, in this case the particular methodology of Besser et al., to arrive at the claimed invention. *In re Lee, 237 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002); Ecolochem Inc. v. Southern California Edison, Co., 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); In re Kotzab, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999).* That burden has not been discharged.

Specifically, as previously pointed out the Examiner's basis for the asserted motivation does not rest upon accurate factual determinations as to the teachings of Mahulikar et al. This is because Mahulikar et al. do not relate to forming openings in a porous dielectric layer leaving a **sidewall** with exposed pores, as no sidewalls in any **porous dielectric layer** are even disclosed, and there is no disclosure of **swelling** any porous dielectric layer. Anodized aluminum cannot be considered a porous dielectric layer regardless of some unintentional defects which may be formed therein.

Further, Appellants note that the type of porous dielectric layer disclosed in the primary reference is a **low dielectric constant material employed in damascene processing. Anodized aluminum is not employed in damascene processing.** Anodized aluminum is not the type of low-k dielectric materials employed by the primary reference to Besser et al. This being the case, it is not apparent and the Examiner has not explained **why** one having ordinary skill in the art would have been **realistically** motivated to **deviate** from the teachings of Besser et al. by looking to sealing techniques in the first place, let alone to look to sealing techniques employed on anodized aluminum which is not

the type of material with which Besser et al. are concerned, and has not been shown to be capable of swelling under the disclosed curing conditions.

The Examiner appears to forget that one having ordinary skill in the art is presumed to follow conventional wisdom and is not prone to invention. *Ecolochem Inc. v. Southern California Edison, Co., supra; Standard Oil Co. v. American Cyanamid Co., 774 F.2d 448, 227 USPQ 293 (Fed. Cir. 1985).* In other words, there is no reason why one having ordinary skill in the art would have been realistically led to experiment with techniques employed to seal different types of materials, such as anodized aluminum, used in packaging vis-à-vis low-k dielectric materials used in damascene processing for forming interconnect structures.

Conclusion.

Based upon the foregoing Appellants submit that the Examiner did not establish a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. § 103 for lack of the requisite factual basis and want of the requisite realistic motivation.

VIII. PRAYER FOR RELIEF

Based upon the arguments submitted *supra*, Appellants submit that the Examiner's rejection under 35 U.S.C. § 103 is factually and legally erroneous. Appellants, therefore, solicit the Honorable Board to reverse the Examiner's rejection of the claims on appeal under 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Arthur J. Steiner
Registration No. 26,106

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 AJS:as/bjs/ntb
Facsimile: 202.756.8087
Date: May 11, 2006

CLAIMS APPENDIX

1. A method of manufacturing a semiconductor device, the method comprising:

forming an opening in a porous dielectric layer comprising a first low-k material overlying a substrate, the opening defined by sidewalls of the porous dielectric layer having exposed pores;

sealing exposed pores in the sidewalls by depositing:

a swelling agent lining the sidewalls and heating to swell the porous dielectric layer; and

depositing a barrier metal layer lining the opening.

2. The method according to claim 1, further comprising:

filling the opening with metal; and

conducting chemical mechanical polishing (CMP) such that an upper surface of the metal filling the opening is substantially coplanar with an upper surface of the porous dielectric layer.

3. The method according to claim 2, comprising:

forming the opening as a dual damascene opening;

filling the opening with copper (Cu) or a Cu alloy as the metal, wherein the porous dielectric layer has a dielectric constant (k) less than 3.5.

8. The method according to claim 1, comprising sealing the pores by:

depositing a swelling agent lining the sidewalls;

heating to swell the porous dielectric layer; and

rinsing with water.

9. The method according to claim 8, comprising heating at a temperature of 25°C to 200°C.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

Not applicable.